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FIG.1

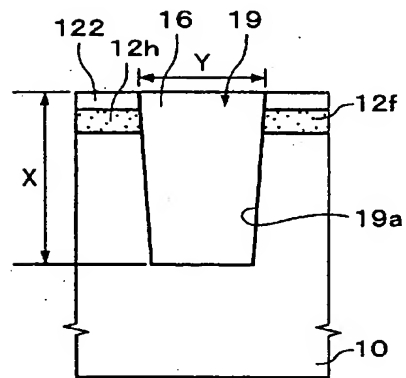
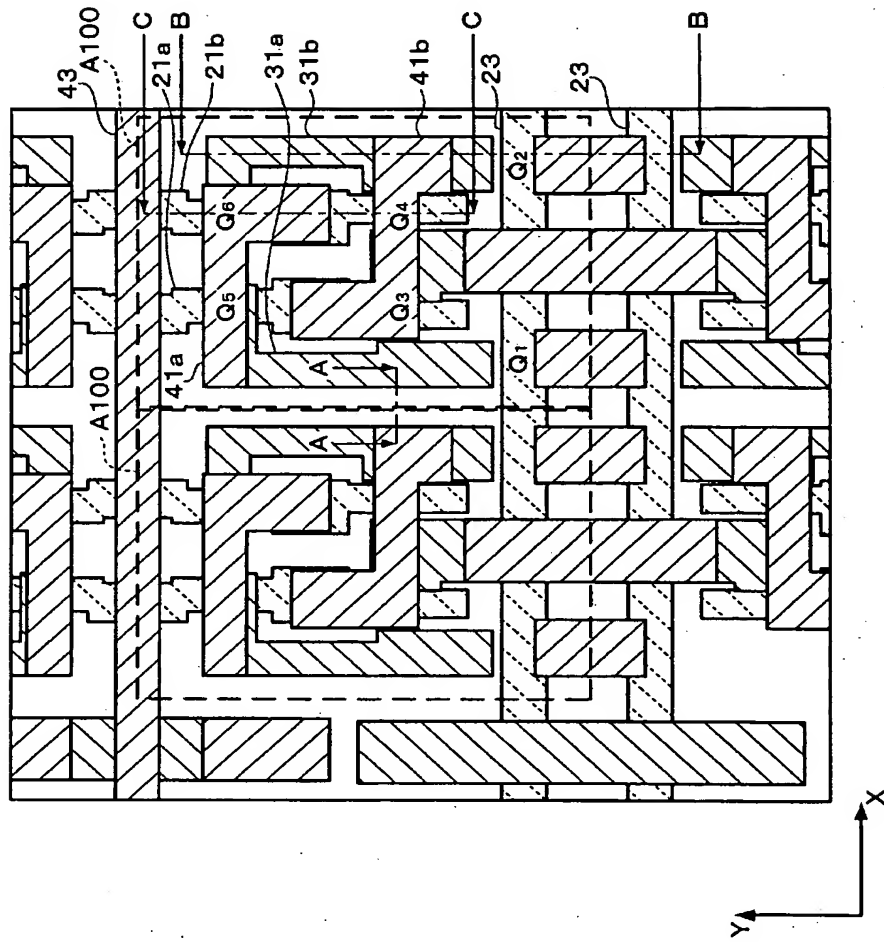
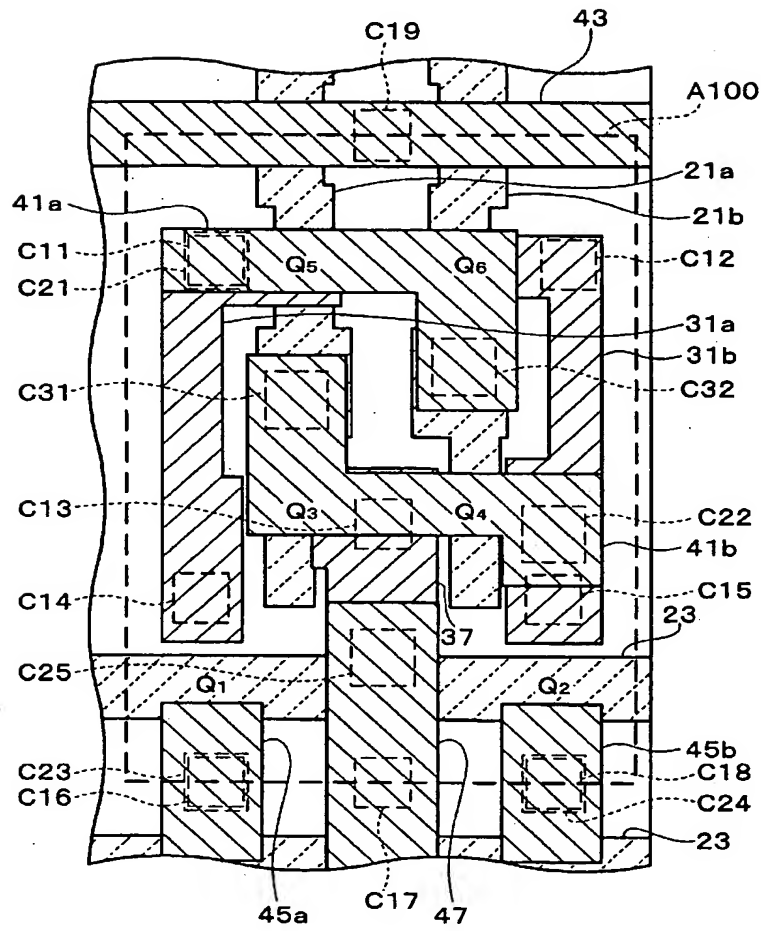


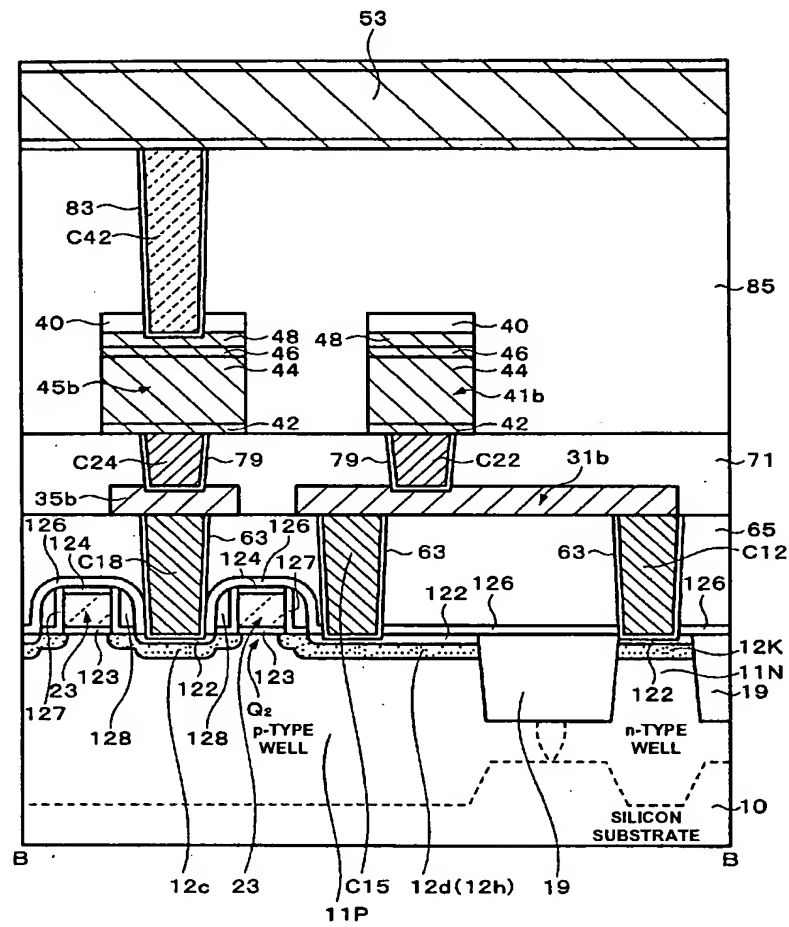
FIG.2



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FIG.3





[illegible]

The diagram shows a single unit cell of a 1T1R1C1 crossbar array. It consists of a central 1T1R1C1 core. The word line (WL) is connected to the gates of the access transistors Q5 and Q6. The bit line (BL) is connected to the source of Q1 and the drain of Q2. The core is connected to VDD and VSS (GND) at the top and bottom, respectively. The core is also connected to the word line (WL) and bit line (BL) at the left and right, respectively.



FIG.8

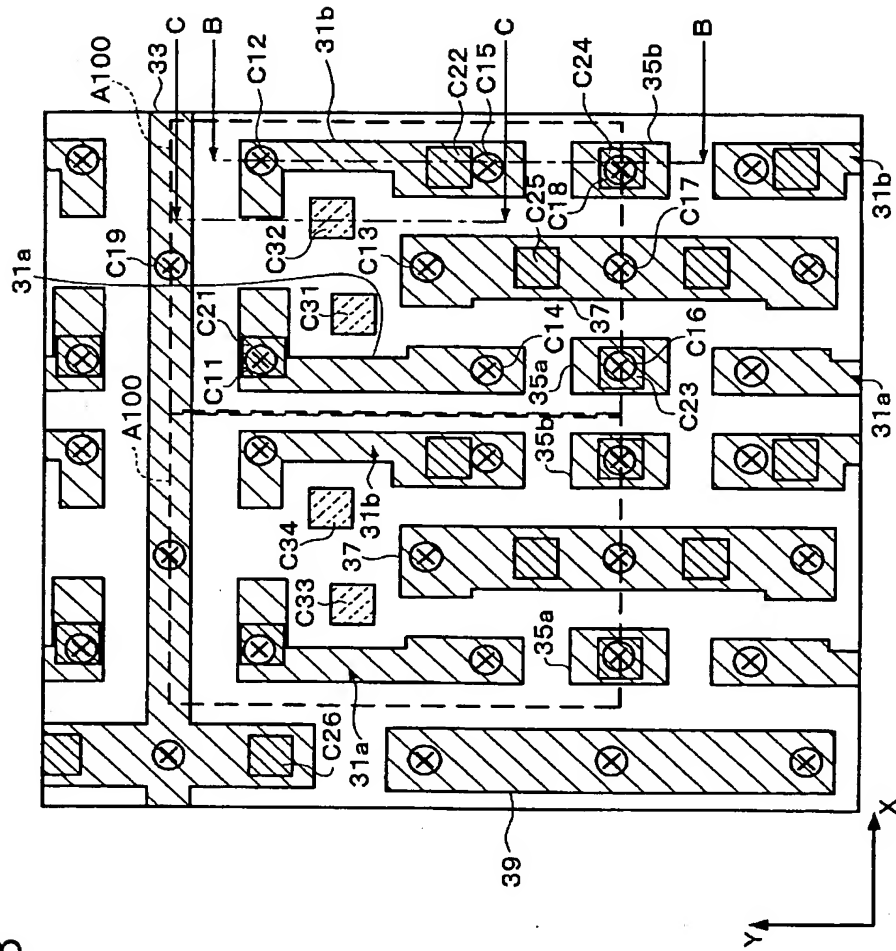


FIG. 9

